IN THE CLAIMS:

Please amend the claims as follows:

1. (Previously Amended) An annealing method of annealing an SOI substrate in a reducing atmosphere, comprising the step of:

holding the SOI substrate by a holding portion having a surface formed from silicon and annealing the SOI substrate, wherein the holding portion is a member having a silicon film thereon or a member formed from single-crystal silicon or polysilicon.

2. (Original) The method according to claim 1, wherein the annealing is executed at a temperature lower than a melting point of single-crystal silicon.

3. (Original) The method according to claim 1, wherein the annealing is executed at a temperature not less than 775°C.

4. (Original) The method according to claim 1, wherein the annealing is executed at a temperature not less than 966°C .

5. (Original) The method according to claim 1, wherein the annealing is executed at a temperature not less than 993°C.

6. (Currently Amended) An SOI substrate manufactured using an annealing method of ~~any one of claims~~ claim 1.

7. (Original) The substrate according to claim 6, wherein an HF defect density is not more than 0.05 defects /cm^2.

8. (Currently Amended) A semiconductor device manufacturing method, comprising the steps of:

annealing an SOI substrate using an annealing method of ~~any one of claims~~ claim 1; and

forming an active region for a transistor in a nonporous semiconductor layer of the SOI substrate.

9. (Canceled)

10. (Original) An annealing method of annealing an SOI substrate in a reducing atmosphere, comprising the step of:

holding the SOI substrate by a holding portion which contains no silicon carbide formed by sintering and has a surface formed from silicon carbide deposited by CVD and annealing the SOI substrate.

11. (Original) The method according to claim 10, wherein the annealing is executed at a temperature lower than a melting point of single-crystal silicon.

12. (Original) The method according to claim 10, wherein the annealing is executed at a temperature not less than 775°C.

13. (Original) The method according to claim 10, wherein the annealing is executed at a temperature not less than 966°C.

14. (Original) The method according to claim 10, wherein the annealing is executed at a temperature not less than 993°C .

15. (Currently Amended) An SOI substrate manufactured using an annealing method of ~~any one of claims~~ claim 10.

16. (Original) The substrate according to claim 15, wherein an HF defect density is not more than 0.05 defects /cm^2.

17. (Currently Amended) A semiconductor device manufacturing method, comprising the steps of:

annealing an SOI substrate using an annealing method of ~~any one of claims~~ claim 10; and

forming an active region for a transistor in a nonporous semiconductor layer of the SOI substrate.

18. (Canceled)